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Spike-based learning with a generalized integrate and fire silicon neuron

Giacomo Indiveri, Fabio Stefanini, and Elisabetta Chicca
Institute of Neuroinformatics
University of Zurich and ETH Zurich
Zurich, Switzerland
Email: giacomo@ini.phys.ethz.ch

***Abstract*— Spike-based learning circuits have been typically used in conjunction with linear integrate-and-fire neurons. As a new class of current-mode conductance-based silicon neurons has been recently developed, it is important to evaluate how the spike-based learning circuits perform, when interfaced to these new types of neuron circuits. Here, we describe a VLSI implementation of a current-mode conductance-based neuron, connected to synaptic circuits with spike-based learning capabilities. The conductance-based silicon neuron has built-in spike-frequency adaptation, refractory period mechanisms, and plasticity eligibility control circuits. The synaptic circuits exhibits realistic dynamics in the post-synaptic currents and comprise local spike-based learning circuits, controlled by the global post-synaptic eligibility circuits.We present experimental results which characterize the conductance-based neuron circuit properties and the spike-based learning circuits connected to it.**

I. Introduction

In 1952 Hodgkin and Huxley developed an extremely accurate and elegant model of biological neurons, based on data from the squid giant axon [1]. It consists of a set of nonlinear ordinary differential equations describing the electrical properties of neurons, where voltage gated ion channels are represented by nonlinear conductances, which change as functions of membrane voltage and time. The H-H model is the most successful and widely-used *conductance-based* model of neurons.

Several VLSI implementations of this and analogous conductance-based models of neurons have been proposed in the past [2]–[5]. However, given their complexity, they require significant silicon real-estate and a large number of bias voltages or currents to configure the circuit properties.

Simplified Integrate-and-Fire (I&F) models would require far less transistors and parameters, but they do not produce a rich cnough rcpcrtoirc of bchaviors uscful for invcstigating the computational properties of large neural networks [6], [7].

This problem has been recently overcome with the proposal of conductance-based or generalized I&F models [6]–[8], that capture many of the properties of biological neurons, but require less and simpler differential equations compared to the H-H model. These types of models have been shown to be efficient both in software simulations and hardware VLSI implementations [6], [9]–[11]. We recently proposed a conductance-based silicon neuron circuit [11] which implements an adaptive exponential I&F model [7]. The circuit is compact, low-power, has biologically realistic time constants, and implements refractory period and spike-frequency adaptation mechanisms which can be used to implement resonances and oscillatory behaviors often emphasized in more complex models [6], [8]. In addition, this circuit is compatible with fast asynchronous Address-Event Representation (AER) logic. This allows us to integrate the neuron circuit in event-based VLSI architectures, and use it to construct large distributed reconfigurable neural networks.

Here we present experimental results from a chip comprising an array of generalized I&F neurons, connected to silicon synapses that exhibit biologically plausible temporal dynamics and spike-driven plasticity [12], [13]. We derive analytically and demonstrate experimentally the silicon neuron's adaptive exponential I&F properties, show how it's adaptation mechanism can be used to implement different spiking behaviors and neural models, and demonstrate how it is compatible with spike-based learning circuits, which have been typically used in conjunction with constant linear I&F circuits in the past [12].

II. The VLSI implementation

The data presented in this paper were measured from a VLSI chip fabricated in a standard 0.35μm, n-well, four metals, double poly, CMOS process. The chip occupies an area of 8.6 mm^2 and comprises a 2.3 mm^2 matrix structure with 32 rows of silicon neurons, each containing 64 synapses.

A. The conductance-based silicon neuron

This circuit, shown in Fig. 1, comprises an input diff-pair integrator (DPI) [14] (M1-M4), which models the neuron's leak conductance and can produce exponential subthreshold dynamics in response to constant input currents. The integrating capacitor C_{mem} represents the neuron's membrane capacitance, while an inverting amplifier (M15-M17) with positive feedback (M11-M14) implements the spike-generation mechanism, modeling Sodium activation and inactivation dynamics. The reset transistor M13 models the Potassium conductance functionality and, together with the constant subthreshold leak transistor M21, implements the refractory-period behavior. A second instance of a DPI (M5-M10), models the neuron's Calcium conductance, and produces an after-hyperpolarizing

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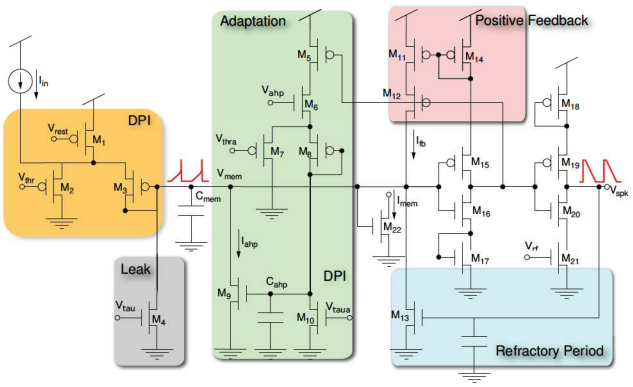


Fig. 1. Schematic diagram of the conductance-based neuron circuit.

current (I_{ahp}) proportional to the neuron's mean firing rate, and responsible for the spike frequency adaptation mechanism.

The equations governing the circuit's subthreshold behavior can be easily obtained by applying Kirchhoff's law on the membrane potential node V_{mem}:

$$C_{mem}\frac{d}{dt}V_{mem} = (I_{dpi} - I_{\tau}) - I_{ahp} + I_{fb} \qquad (1)$$

where $I_{dpi} = I_{M3}$, $I_{\tau} = I_{M4}$, $I_{ahp} = I_{M9}$, and the positive feedback current I_{fb} is

$$I_{fb} = I_0^{\frac{1}{\kappa+1}} I_{mem}^{\frac{\kappa}{\kappa+1}} \frac{1}{1+e^{-\alpha(I_{mem}-I_{th})}}. \qquad (2)$$

The α and I_{th} parameters in eq. (2) are related to the inverter's gain and switching point, and depend on layout and process parameters.

By applying a current-mode analysis for both the input and spike-frequency adaptation DPI circuits [11], [14] to eq. (1) we obtain:

$$\begin{cases} \tau \frac{d}{dt} I_{mem} & = \frac{I_{mem}}{I_{\tau}} \left(\frac{I_{in}}{1+\frac{I_{mem}}{I_g}} - I_{\tau} + I_{fb} - I_{ahp} \right) \\ \tau \frac{d}{dt} I_{ahp} & = \frac{I_{ahp}}{I_{\tau_a}} \left(\frac{I_{spk}}{1+\frac{I_{ahp}}{I_{g_a}}} - I_{\tau_a} \right) \end{cases} \qquad (3)$$

where I_{mem} is the subthreshold current flowing through the output n-FET M22, the current I_{spk} is equivalent to the current flowing through M6 I_{M6} during a spike, $I_{tau_a} = I_{M10}$, and the terms τ, I_g, τ_a, and I_{g_a} are defined as:

$$\tau \triangleq \frac{CU_T}{\kappa I_{\tau}} \qquad I_g \triangleq I_0 e^{\frac{\kappa}{U_T} V_{thr}}$$
$$\tau_a \triangleq \frac{C_{ahp} U_T}{\kappa I_{\tau_a}} \qquad I_{g_a} \triangleq I_0 e^{\frac{\kappa}{U_T} V_{thr_a}}$$

If we set the two threshold voltages to zero, and assume that $I_g \ll I_{mem}$, and $I_{g_a} \ll I_{ahp}$, the coupled non-linear differential equations in eq. (3) simplify to:

$$\begin{cases} \tau \frac{d}{dt} I_{mem} + I_{mem} & \approx \frac{I_g I_{in}}{I_{\tau}} - \frac{I_{mem} I_{ahp}}{I_{\tau}} + f(I_{mem}) \\ \tau \frac{d}{dt} I_{ahp} + I_{ahp} & \approx \frac{I_{g_a} I_{spk}}{I_{\tau_a}} \end{cases} \qquad (4)$$

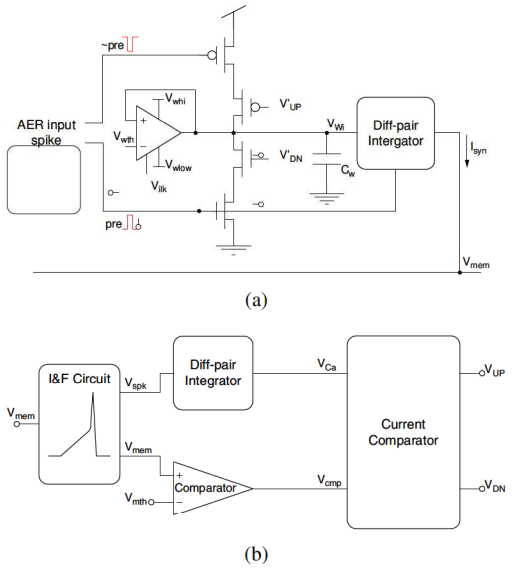


Fig. 2. Spike based learning circuit diagrams. (a) Presynaptic weight update module (one per plastic synapse). Upon the arrival of a pre-synaptic input spike, the circuit in (a) updates the synaptic weight V_w, according the V_{UP} and V_{DN} eligibility traces produced by the circuits in (b). The positive-feedback amplifier has a very long slew-rate, and slowly drives the weight V_w to one of two stable states (V_{whi} and V_{wlow}) depending if the updates pushed V_w above or below the threshold V_{wth} (bistability circuit). The DPI circuit in (a) produces post-synaptic currents that are summed at the soma's V_{mem} node.(b) Post-synaptic eligibility circuits (one per neuron). The post-synaptic spikes are integrated by a DPI and produce a current I_{Ca} proportional to its mean firing rate. A voltage comparator compares the post-synaptic neuron's membrane potential V_{mem} to a V_{mth} threshold. If $V_{mem} > V_{mth}$ this block selects weight increases (via V_{UP}), otherwise it switches to weight decreases (via V_{DN}). The current comparator compares the I_{Ca} current to constant threshold biases, and determines weather to allow the up/down jumps or to disable the weight updates (*i.e. stop-learning*). If I_{Ca} is in an intermediate range between these thresholds, one of the two eligibility traces V_{UP} or V_{DN} is activated. Otherwise, they are both set to the respective supply rails (see [13] for a detailed description).

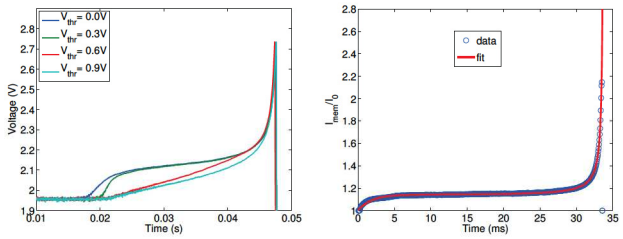
where the $f(I_{mem}) = I_{mem} I_{fb}/I_{\tau}$ represents the positive-feedback contribution and exhibits, to first order approximation, an exponential dependence with I_{mem}.

Therefore the circuit of Fig. 1, described by eq. (4) represents a generalized I&F conductance-based model, which has the specific form of an adaptive *exponential* I&F model [7]. The spike-triggered adaptation current I_{ahp} has the same effect as described in the Izhikevich and analogous models [6], [7]. So depending on the values of the parameters chosen, the neuron circuit presented can be tuned to reproduce qualitatively a large variety of classes of neurons.

In Section III-A we will present data measured from the neuron circuit which demonstrates the circuit's conductance-based and positive feedback properties, and show an example in which the adaptation current has been tuned to produce bursting.

B. The spike-based learning synapse

Plasticity mechanisms based on the timing of the spikes can be mapped very effectively onto silicon neuromorphic devices [15]–[17]. We recently implemented a spike-driven



(a) (b)

Fig. 3. Silicon neuron response to a constant input current. (a) Range of different model behaviors as a function of the V_{thr} parameter (going from conductance-based to constant linear I&F). In order to plot all measurements on the same scale, the input currents were adjusted to compensate for the changes in gain induced by the V_{thr} variations. (b) Fit of circuit response with eq. (5).

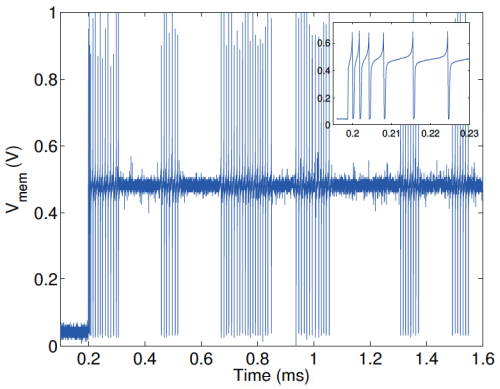


Fig. 4. Circuit response to a step input current, with spike frequency adaptation mechanism enabled and parameters tuned to produce bursting behavior. The figure inset represents a zoom of the data showing the first 6 spikes.

learning rule, originally proposed in [18], and demonstrated how it is extremely robust and powerful for classifying patterns of mean firing rates [13]. The learning circuits were interfaced however to the linear I&F circuits used in the past. We used the same model to implement plastic excitatory synapses of the chip presented in this paper. Figure 2 describes these circuits and their operating principles.

In the Section III-B we demonstrate how the new neuron circuit is compatible with these learning circuits, and present an example of Long-Term-Depression (LTD), in which the synapse is trained to reduce its weight.

III. Experimental Results

A. Silicon neuron measurements

As explained in Section II-A, the non-linear differential equations in eq. (3) can be reduced to first-order linear differential equations, depending on the value of V_{thr} (see Fig. 1). We injected constant current in the neuron and recorded the membrane potential, for 4 different values of V_{thr}. Figure 3(a) shows the effect of the V_{thr} changes, demonstrating how it is possible to smoothly go from a constant linear I&F behavior ($V_{thr} = 0.9V$) to a conductance-based one ($V_{thr} = 0V$).

To fit the $I_{mem}(t)$ data measured from the neuron circuit, we derived the following function, from eq. (4), assuming $I_{ahp} = 0$:

$$I_{mem}(t) = I_0 + \frac{I_g I_{in}}{I_\tau}(1 - e^{-t/\tau}) + I_{fb0}\left(\frac{e^{\alpha(t-t_0)}}{1 + \beta e^{\alpha(t-t_0)}}\right) \quad (5)$$

where I_{fb0}, t_0, α, and β are free fitting parameters. As shown in Fig. 3(b) the fit is extremely accurate over the full subthreshold response range.

To show the effect of the spike-frequency adaptation mechanism, we set the relevant bias voltages to appropriate values, applied a step change in input with a constant input current, and measured the neuron's membrane potential V_{mem} in response to that. Figure 4 shows an example in which we set $V_{tau_a} = 0.05V$, $V_{thr_a} = 0.14V$, $V_{ahp} = 2.85V$. As shown, we were able to tune the adaptation circuits in a way to produce bursting behavior. This was achieved by simply increasing the gain of the negative feedback adaptation mechanism ($V_{thr_a} > 0$). In control-theory terms, this is equivalent to going from an asymptotically stable regime to a marginally stable one, that produces ringing in the adaptation current I_{ahp}, which in turn produces bursts in the neuron's output firing rate. This was possible due to the flexibility of the DPI circuits used, which allow us to take advantage of the extra control parameter (V_{thr_a}, in addition to V_{ahp}) and the possibility of exploiting its non-linear transfer function (see eq. (3)), without requiring special tricks or dedicated resources that alternative neuron models have to use [8]–[10].

B. Spike-based learning measurements

One of the key characteristics that distinguishes the spike-driven learning mechanism implemented in this chip, from the vast majority of other spike-driven or Spike Timing Dependent Plasticity (STDP) learning mechanisms proposed in the literature is its *stop-learning* feature [18]. Synaptic weights are updated only if the neuron's response to the input pattern is ambiguous: if the input patterns presented to the neuron's synaptic array produce a (weighted, summed) net input current which drives the neuron to fire either very strongly or weakly, then no further learning occurs (the stop learning condition is met), as it is assumed that the input pattern is successfully classified. If on the other hand the neuron produces an intermediate mean output firing rate (ambiguous classification result), then weight updates are allowed and occur following the rule defined in [18].

In Fig. 5 we show an experiment where we stimulated a plastic synapse with pre-synaptic Poisson distributed spikes, using bias parameters that produce weight updates only for sufficiently high post-synaptic mean output firing rates. The weight was initially set to a high stable state, such that pre-synaptic input spikes could drive the neuron to produce post-synaptic output spikes, and the circuits were configured to produce only downward weight updates. Figure 5 shows an example in which learning is stopped if the post-synaptic activity is too low (*i.e.* if V_{Ca} drops below a set threshold). When learning does occur, pre-synaptic input spikes induce

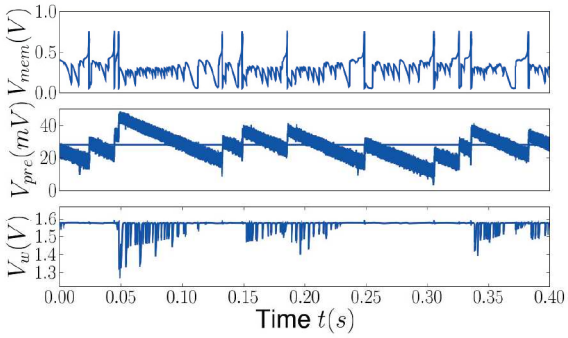
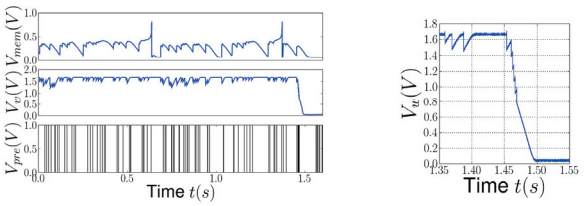


Fig. 5. Stop-learning and weight updates. The top trace shows the post-synaptic membrane potential; the middle trace shows the neuron's mean firing rate (encoded in the V_{Ca} voltage of Fig. 2(b)); the bottom trace shows the synaptic weight value. Bias parameters were set so that learning would stop when V_{Ca} dropped below the set threshold.



(a) (b)

Fig. 6. Long-Term Depression (LTD) transition. (a) Pre-synaptic input spikes (bottom trace) induce downward jumps in the synaptic weight (middle trace) when the right conditions are met by the post-synaptic membrane potential (top trace). The spikes eventually drives the weight below the bistability threshold at approximately $t = 1.5s$. (b) Zoom of the synaptic weight voltage around the transition time.

downward jumps in the V_w voltage, while the bistability circuit drives the weight back toward its high stable state. If a sufficient number of downward jumps drives the V_w voltage below the bistability threshold V_{wth}, then the synapse "learns" an LTD transitions, the bistability circuit switches polarity, and the weight is driven toward its low stable state. This is shown in Fig. 6, where The LTD transition occurs around $1.45s < t < 1.5s$, when a burst of pre-synaptic spikes decreases V_w significantly (see Fig. 6(b)).

A comprehensive description of these spike-driven learning circuits, and of their (robust) performance characteristics is provided in [13].

IV. Conclusion

We presented a novel conductance-based generalized I&F neuron circuit, derived its response properties analytically and demonstrated its features experimentally. We showed how it is compatible with spike-driven learning circuits and presented preliminary results that demonstrate stop-learning and LTD capabilities. As these neuron and synapse circuits are integrated in multi-neuron AER chips, we plan to investigate spike-driven computation and learning properties at the network level, and apply these devices for event-driven classification and recognition tasks.

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